An Overview of Frequency Synthesizers for Radars

Zvi Galani, *Senior Member, IEEE*, and Richard A. Campbell

Abstract —**This paper presents an overview of frequency synthesizer techniques suitable for radar systems. Included are the requirements which have a direct impact on the selection of synthesizer architectures and the choice of synthesizer components. Both direct and indirect architectures are presented, along with advantages, disadvantages, and representative examples. A brief discussion of analytical procedures is followed by a survey of key synthesizer components and future trends.**

I. Introduction

The use of frequency synthesizers in test equipment, radar, and communication systems has been growing steadily because of their many advantages, especially frequency selection with digital commands and predictable frequency stability. Although all synthesizers share common features, they also exhibit significant differences as a result of specific system requirements and/or specific applications.

Radar synthesizers often have more stringent noise and spurious signal requirements than the other types, primarily because they are used as the timing reference between the transmitted and the received signals of the radar.

This paper presents various synthesizer architectures and key synthesizer components, along with a discussion of advantages and disadvantages. Some architectures are hardware intensive and, because of their physical size, are more suitable for stationary or shipboard radars. Architectures requiring smaller volume are more suitable for airborne applications.

Direct, phase-locked, and frequency-locked architectures are covered, including key building blocks and performance limitations. The direct digital synthesizer (DDS) architecture is considered briefly, as it is not yet widely used in radar systems. Finally, projections are made of advances in components that have a direct effect on frequency synthesis.

II. Requirements

The electrical requirements of a frequency synthesizer are derived from the radar system performance requirements, just as its mechanical requirements reflect those of the radar. The major requirement categories are listed below.

Manuscript received July 13, 1990; revised November 20, 1990.
Z. Galani is with the Missile Systems Division, Raytheon Company, Hartwell Road, Bedford, MA 01730.
R. A. Campbell is with the Missile Systems Division, Raytheon Company, 50 Apple Hill Drive, Tewksbury, MA 01876.
IEEE Log Number 9143000.

A. Electrical Requirements

1) Frequency Format: The frequency format (total bandwidth, frequency spacing, etc.) is usually well defined by the requirements of the radar system. Occasionally there is a requirement for a specific pattern of frequencies versus time, but usually only frequency agility is required, i.e., a specific frequency upon command.

2) Frequency Switching Time: Frequency switching time represents one of the driving requirements of various synthesizer architectures. While communication system and test equipment applications can usually perform adequately with millisecond frequency switching, radars often require microsecond switching. Fast switching has a definite impact upon radar synthesizer design, because it eliminates from consideration closed-loop architectures with long frequency switching and settling times.

3) Noise: Some radars, such as airborne ground avoidance systems, have modest noise requirements. The noise allocation of high-performance radars can be as much as 70 dB lower, with all levels in between specified for other radar types. Amplitude noise levels are rarely as critical as phase noise since the amplitude noise can be reduced by balanced mixers, amplifiers in compression, or diode limiters. Phase noise close to the carrier, however, can be reduced only with either lower noise oscillators or with external closed-loop circuits. In most cases the net effect of amplitude noise is to add to the effective receiver noise level, but in applications involving nonlinear circuits, such as amplifiers in compression, some of the amplitude noise is converted to phase noise.

4) Spurious Signals: Spurious signals either mask the radar returns or create false targets.

5) Long-Term Frequency Stability: In some radar applications long-term frequency stability is not as stringent as in communication systems, for when the same source determines both the transmission and the reception frequencies in a radar, a small amount of frequency drift is allowable. However, the absolute frequency must be controlled in radars requiring long integration times or radars that interact with other independent systems.

6) Modulation: Modulation of radar signals is usually well defined in time, amplitude, and frequency. The typi-

0018-9480/91/0500-0782$01.00

cal modulation waveform has a fixed pattern in amplitude and frequency. Amplitude modulation and low-deviation phase modulation can be added following signal generation, but frequency-modulated signals with large indices must be generated by the oscillator.

B. Mechanical Requirements

The mechanical design of frequency synthesizers is influenced mainly by volume constraints and shielding requirements. While synthesizers for stationary radars have minimal volume constraints, synthesizers for airborne applications, especially missiles, are designed to very rigidly defined form factors and weight limits which usually require some level of miniaturization. The degree of shielding needed in a synthesizer depends on the architecture, the allowable spurious levels, and EMI/EMC considerations.

Environmental conditions such as temperature extremes and vibration also have a significant impact on both electrical and mechanical designs of a synthesizer. Temperature extremes dictate the extent of the worst-case electrical design, thermal design, and the choice of appropriate materials. Vibration levels dictate the integrity of the mechanical design and use of resilient mounts for potentially microphonic components. In the case of indirect synthesizers, they also dictate the use of loops with wider bandwidth to reduce oscillator phase noise under vibration.

III. Frequency Synthesizer Architectures

Usually an initial investigation of the specifications leads to the class of synthesizer architectures best suited for a given application. The choice is based upon such parameters as the number of frequencies, frequency spacing, frequency switching time, noise, spurious levels, volume constraints, and cost. The various classes of synthesizer architectures along with their essential characteristics are presented below.

A. Direct Frequency Synthesizers

This class of architectures creates its output frequency by mixing two or more signals to produce sum or difference frequencies, by frequency multiplication, by frequency division, or by any combination thereof. The most widely used components are reference oscillators, frequency multipliers, frequency dividers, mixers, filters, and switches.

The key advantages of direct synthesizers are fast frequency switching and the capability of some architectures to generate signals with very low phase noise. This low-noise performance is achieved by the selection of topologies and components such that the additive phase noise of all the components is considerably smaller than the multiplied phase noise of the reference oscillators which determine the output phase noise of the synthesizer. The disadvantages of direct synthesizers are that they are hardware intensive and tend to generate an excessive number of spurious signals.

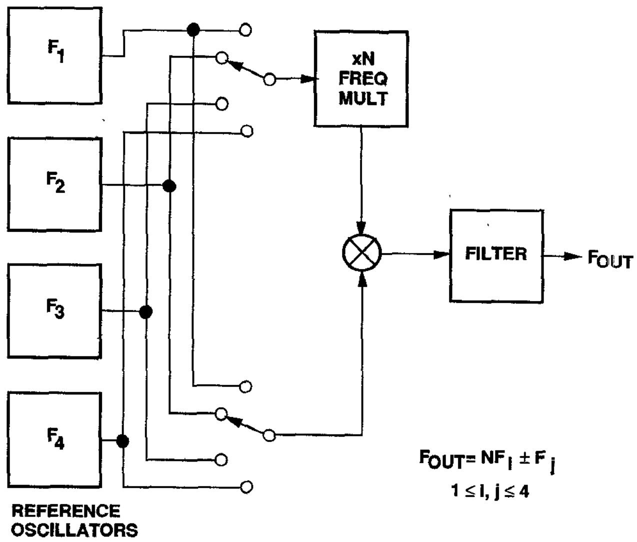


Fig. 1. Direct frequency synthesizer block diagram.

The various forms of direct synthesizers differ in the way their sets of frequencies are generated and in the number and organization of their mixers. The sets may be individual oscillators or synthesized frequencies themselves. Mixers can be organized in series (the number of output frequencies being the product of the number of frequencies in the sets) or in parallel (for multiple frequency generation) or any combination thereof. The synthesizer can be described mathematically, wherein mixing is represented by addition or subtraction and harmonics (or subharmonics) by multiplication (or division).

The exact form of a synthesizer is driven first by its gross features (number of frequencies, noise, etc.) and second by its spurious signal generation. The subject of spurious signals is considered in some detail in a subsequent section of this paper.

One direct frequency synthesizer capable of low-noise performance is shown in the block diagram of Fig. 1. It consists of a set of signal sources that are used twice to generate the output frequency. One source is selected and sent to a frequency multiplier, and then to the mixer. The second signal to the mixer is another (or the same) source used directly. The output is the sum (or difference) of these two, yielding 16 frequencies at the output for a set of four sources. Variations on this concept would include the use of more than one multiplier and the use of multipliers in the direct path. An equivalent architecture could use frequency dividers such that the direct and divided paths to the mixer would produce the same result, provided the source frequencies were appropriately higher. This technique is often used to synthesize frequencies with spacings that are smaller than the reference frequency spacings.

Another low-noise direct synthesizer architecture is presented in Fig. 2. Here three sets of signal sources are used to generate 100 frequencies. One set has four fre-

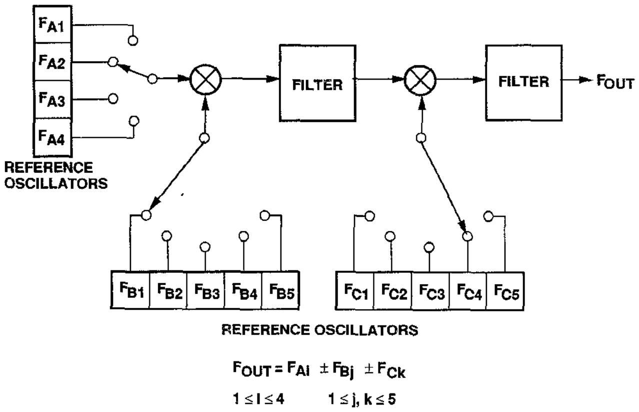


Fig. 2. Direct frequency synthesizer block diagram.

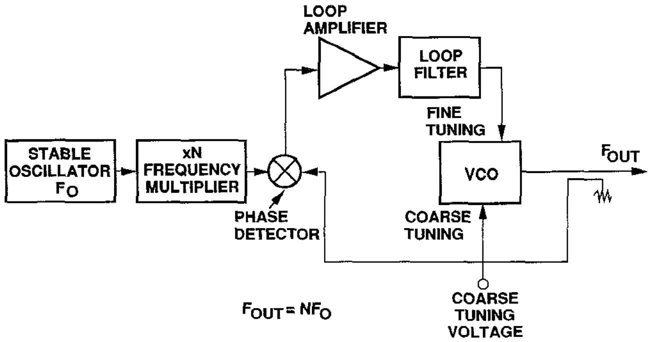


Fig. 3. Analog phase-lock loop block diagram.

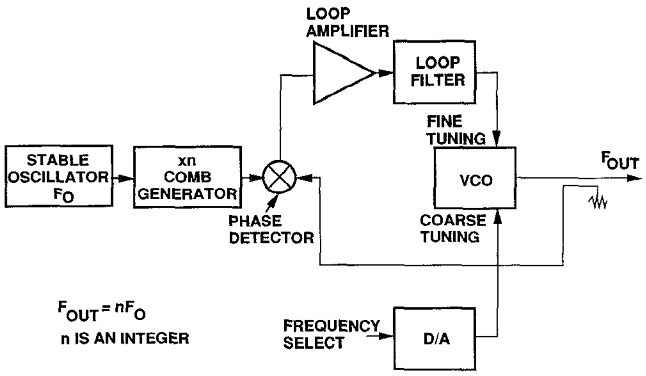


Fig. 4. Block diagram of an analog indirect frequency synthesizer with a comb generator reference.

quencies while the other two have five. If the frequencies are chosen so that the output frequencies of the mixers are the difference between the input frequencies, then spurious signals with in-band frequencies caused by mixer intermodulation products are minimized.

In any synthesizer architecture, the sources could all be oscillators, either free-running or phase-locked to a common reference to achieve coherent operation, or CW signals generated by direct or indirect means. Coherency, especially with respect to a radar's pulse repetition rate, can reduce the effects of many spurious signals.

Many other direct synthesizer architectures are in existence and are described in the literature [1]–[3]. A significant number of these architectures are not suitable for radar applications because of insufficiently low noise and/or spurious signal levels.

B. Direct Digital Synthesizers

The DDS is the most recent addition to frequency synthesis architectures [1], [3], [4]. In response to digital commands, an accumulator generates a digital approximation of a linearly increasing phase function, at a rate controlled by a reference oscillator. The output of the accumulator is applied to a read-only-memory (ROM) look-up table which converts the phase samples into samples of a sinusoidal waveform. The ROM output is fed into a digital-to-analog (D/A) converter which generates an analog approximation of the sinusoidal waveform which, after filtering by a low-pass filter, is the output of the synthesizer.

The main advantages of the DDS architecture are fast and phase-continuous frequency switching, arbitrarily small frequency spacing, small size, and low cost. Its main disadvantages are a limited operating frequency and relatively high noise and spurious signal levels.

C. Indirect Frequency Synthesizers

Indirect frequency synthesizers serve a useful purpose in applications where very fast frequency switching and extremely low noise performance are not required. Indirect synthesizer architectures fall into two broad categories: analog and digital. Combinations of the two are also used in some applications. The fundamental building blocks of analog indirect synthesizers are either frequency-lock loops (FLL's) [5] or analog phase-lock loops (PLL's) [1], [4], [6] while digital indirect synthesizers comprise digital PLL's [1], [4], [6].

1) Analog PLL Synthesizers: A block diagram of a basic analog PLL is presented in Fig. 3, in which a voltage-controlled oscillator (VCO) is phase-locked to a reference signal. Typically, the reference frequency is generated by a stable oscillator followed by a frequency multiplier. In this diagram a portion of the VCO signal and the reference signal are the inputs to the phase detector. The output signal of the phase detector, representing the error signal, is amplified, filtered, and applied to the fine-tuning port of the VCO. Inside the loop bandwidth the phase noise of the VCO is reduced by the open-loop gain to a level limited by the phase noise of the reference. Frequency acquisition is accomplished by applying a voltage to the coarse-tuning port of the VCO to slew its frequency into the capture range of the PLL.

A frequency synthesizer based on an analog PLL with output frequencies corresponding to selected harmonics of a stable frequency is shown in Fig. 4. Here the reference frequency is generated by a stable oscillator followed by a comb generator. Frequency switching is performed by applying a voltage to the coarse-tuning port of the

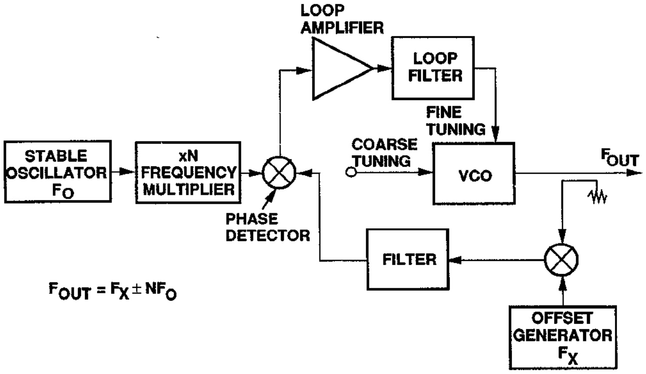


Fig. 5. Single-offset analog phase-lock loop block diagram.

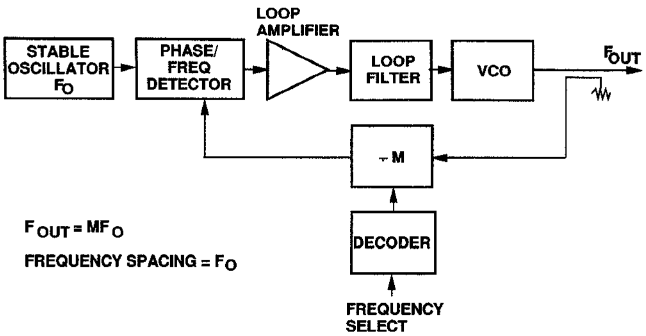


Fig. 6. Digital indirect frequency synthesizer block diagram.

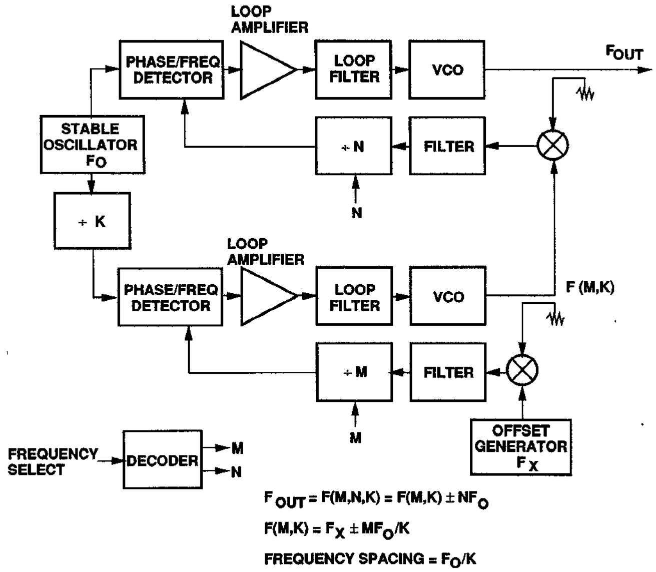


Fig. 7. Block diagram of a two-loop digital indirect frequency synthesizer.

VCO and either opening the loop or slewing the voltage at a rate that is faster than the loop can follow, to prevent the loop from inhibiting the frequency change. An alternative method of reference frequency generation could use a bank of switched stable oscillators followed by frequency multipliers.

Offset PLL's offer another method of frequency synthesis. A block diagram of a single-offset analog PLL is shown in Fig. 5. Here the VCO frequency is heterodyned to a lower frequency using the signal of an offset generator. Frequency agility can be achieved with a multifrequency offset generator in conjunction with a fixed-frequency or a multifrequency reference. An arbitrary frequency resolution can be realized by successively heterodyning the VCO frequency with several multifrequency offset generators with successively finer frequency resolution. In cases where the multifrequency offset generators are indirect frequency synthesizers, the resultant is a multiloop architecture.

The phase noise (inside the loop bandwidth) of the architectures in Figs. 3 and 4 is usually determined by the VCO noise, the open-loop gain, and the phase noise of the reference. In the case of the architecture in Fig. 5, it could be influenced also by the phase noise of the offset generator.

2) Digital PLL Synthesizers: A block diagram of a basic digital indirect synthesizer (based on a digital PLL) is shown in Fig. 6. Here the VCO is phase-locked to a harmonic of the reference frequency, the harmonic order being equal to the division ratio of the digital frequency divider. Synthesis of equally spaced frequencies (frequency spacing equal to the reference frequency) is performed using a programmable digital frequency divider, with all the frequencies synthesized by programming suitable division ratios. The operation of this PLL is similar to that in Fig. 3 except that here phase detection is performed at a reference frequency which is a subharmonic of the VCO frequency. The frequency is switched with a digital command that changes the frequency division ratio and causes the loop to unlock. Under these conditions the phase/frequency detector generates a frequency-dependent voltage which, following amplification and filtering, slews the frequency of the VCO to the lock frequency. In some applications, external frequency acquisition aids are added to reduce the frequency switching time. In the block diagram of Fig. 6 the phase noise of the VCO (inside the loop bandwidth) can be reduced by the open-loop gain to a level that is limited by the multiplied cumulative noise of the reference, the phase/frequency detector, the digital divider, and the loop amplifier. Therefore, large frequency division ratios cannot be used in low noise applications.

Offset digital PLL's are usually limited to a single offset because of the presence of the digital frequency dividers. Such PLL's are used in applications where the VCO frequency exceeds the highest operating frequency of the programmable frequency divider and the phase noise requirements preclude the use of a high-frequency prescaler (fixed-division-ratio frequency divider) because it increases the frequency division ratios.

In low-noise applications requiring synthesis of a large number of frequencies, multiple-loop architectures are used to reduce the maximum frequency division ratio and the number of ratios that otherwise would be necessary. In the two-loop synthesizer shown in Fig. 7 an auxiliary

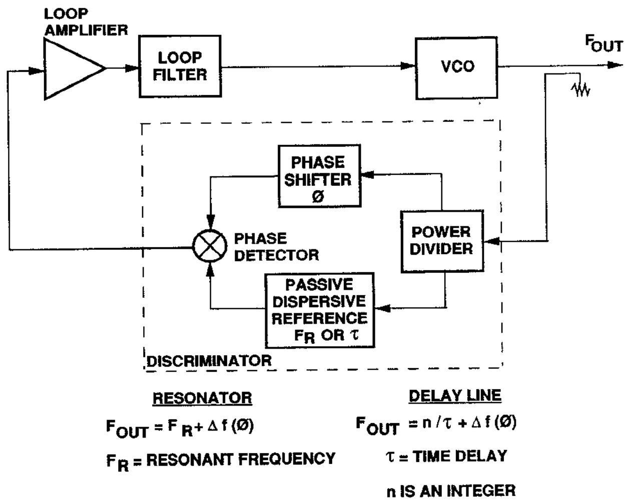


Fig. 8. Frequency-lock loop block diagram.

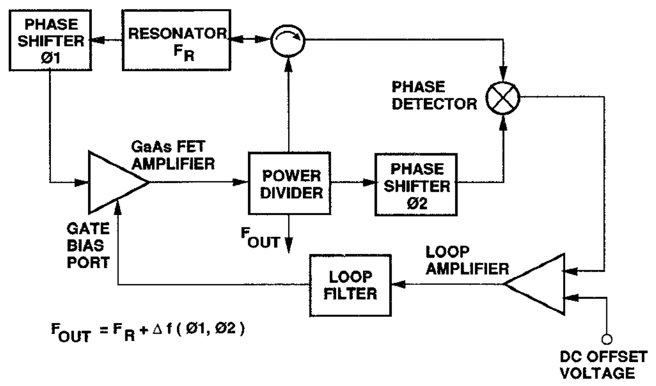


Fig. 9. Block diagram of a single-resonator oscillator and frequency-lock loop.

loop is used to synthesize offset frequencies for the main loop. To synthesize 100 equally spaced frequencies the architecture in Fig. 6 would require 100 consecutive frequency division ratios while the architecture in Fig. 7 could have ten consecutive frequency division ratios in each loop. For example, if the division ratios in Fig. 6 ranged from 101 to 200, then inside the loop bandwidth the cumulative phase noise at the reference frequency would be enhanced by as much as 46 dB (20 log N). In Fig. 7, on the other hand, using $K = 10$, the lower loop would have division ratios (M) from 11 to 20, which results in maximum noise enhancement of 26 dB. The upper loop would therefore have ratios (N) from 1 to 10, which cause 20 dB maximum noise enhancement. The total noise enhancement is 27 dB because the output noise is the statistical sum of the enhanced noise and the noise of the offset signal.

3) FLL Synthesizers: Frequency-lock loops (FLL's) offer another method of indirect frequency synthesis. The major difference between a PLL and a FLL is that the frequency stability of a PLL is related to that of a reference oscillator while the frequency stability of a FLL is related to the phase stability of a passive dispersive element in the discriminator, such as a resonator or a delay line. In the block diagram of a typical FLL shown in Fig. 8, a portion of the VCO output signal is applied to the input of a discriminator. Variations in the VCO output frequency are converted to voltage variations which are amplified, filtered, and fed to the fine-tuning port of the VCO to reduce these frequency variations. The phase noise realizable with a FLL inside the loop bandwidth is dependent on the VCO noise, the open-loop gain, and the additive phase noise of the loop components. In applications requiring the use of narrow-band PLL's, wide-band phase noise reduction can be obtained by the addition of a tunable FLL.

One approach to frequency synthesis is with a FLL using a delay line in the discriminator [7]. The frequency response of a delay line discriminator is periodic, with every other zero crossing corresponding to a stable VCO frequency. Similar to an analog PLL, the frequency is switched by applying a voltage to the coarse-tuning port of the VCO to slew the frequency into the capture range about the selected frequency.

A unique FLL is presented in Fig. 9, where the resonator serves a dual function as the frequency determining element of the oscillator and as the dispersive element of the discriminator. Because of this feature, the circuit does not need external frequency acquisition aids [8].

4) Advantages and Disadvantages of Indirect Synthesizers: The major advantages of indirect frequency synthesizers are reduced levels of spurious signals owing to the low-pass filter action of the loop, and lower level of complexity with smaller volume compared with direct synthesizers. The main disadvantages of indirect synthesizers are longer frequency switching time (which increases with a decrease in loop bandwidth) and higher phase noise compared with direct synthesizers.

An advantage of both FLL's and analog PLL's is that they have the lowest phase noise achievable with indirect synthesizers because phase detection is performed at the VCO frequency. Their disadvantage is the need for external frequency acquisition aids.

An advantage of the indirect digital architecture is that it does not require external frequency acquisition aids. Its disadvantage is that, inside the loop bandwidth, the phase noise is determined not only by the multiplied phase noise of the reference but also by the multiplied phase noise of the phase/frequency detector, the loop amplifier, and the digital frequency divider.

IV. Analysis

A candidate synthesizer model can be subjected to a mathematical analysis in order to determine its predicted performance [1], [4]–[6]. The gross features (number of frequencies, etc.) are covered in the initial design, but spurious signals and noise levels are not so obvious. As these are influenced by the various filters in the synthesizer, it is necessary to specify them before analyses can be performed.

A. Spurious Signal Analysis

The design process for a direct synthesizer architecture is sometimes a series of alternating architecture selections and spurious signal analyses. In this case the filter, or bank of filters, following the mixer greatly influences the results. Spurious signal analysis is the primary tool in fixing the final architecture, and should be done early in the design process, for if excessive spurious signals are generated, it is almost impossible to reduce them after the circuits are built.

The actual analysis is accomplished by calculating spurious frequencies with the formula $|mF1 + / - nF2|$, where m and n are integers $0, 1, 2, 3 \cdots$, and $F1$ and $F2$ are the input frequencies to a mixer. Alternatively, spurious frequencies can also be the various harmonics of the source frequency at the output of a frequency multiplier. The expected level of a mixer spurious signal can be determined from many published tables of mixer intermodulation products [9]. Attenuation from filters should also be included in prediction of spurious levels. If the levels are too high, other sets of frequencies must be found or a new architecture must be selected.

In indirect synthesizers a PLL has fewer unwanted mixer products, but is subject to the reference signal feeding through to the VCO, especially for offset and digital PLL's which have lower frequency reference signals. Additional attenuation of the reference signal can be obtained by reducing loop bandwidth, but this must be traded off against the longer settling time of the loop. In offset PLL's there can be a direct leakage of the offset frequency to the VCO output circuitry through the first mixer in the feedback loop. Isolators must be put into the signal path from the VCO output circuitry to the mixer in order to reduce this leakage.

Other sources of spurious signals include an inadequate on/off ratio in switches used to select the desired frequency in direct synthesizers. The frequencies of a set that are not selected generate spurious signals in the band of the synthesizer. Moreover, the power level of any spurious signal is increased by as much as the square of any frequency multiplication factor involved, necessitating higher on/off ratios for switches preceding frequency multipliers.

Spurious signal sources that are not a result of the synthesis process itself include signal leakage paths around filters and switches, either direct physical coupling of input to output, or through auxiliary circuits such as switch driver or power supply leads. These leakage paths do not greatly influence synthesizer design but can have an effect on its physical layout.

B. Noise Analysis

A noise analysis will point out if the proper types of circuit elements have been chosen. For example, field-effect transistor (FET) amplifiers are noisier than bipolar amplifiers, although the noisier amplifier must sometimes be used, such as at frequencies above Ku band. The two most important elements in determining noise performance are the type of reference oscillator and the multiplication factor used, and whether the PLL's, if any, will degrade the phase noise levels (by either having too much VCO noise, not enough open-loop gain, not enough loop bandwidth, etc.). Noise analyses are usually done once early in the design and then are repeated after the circuits are nearly finalized.

V. Frequency Synthesizer Components

The choice of the individual components greatly influences synthesizer performance. Mature components such as switches and filters are well known and do not require special consideration. Other components such as VCO's, frequency multipliers, and frequency dividers merit attention and are covered in the following brief survey.

A. Voltage-Controlled Oscillators

Most VCO's utilize solid-state devices such as bipolar transistors, FET's, Gunn diodes, and IMPATT diodes. Gunn and IMPATT diodes are used mainly at millimeter-wave frequencies, which are beyond the operating frequency range of transistors. VCO circuits can be divided into two broad categories: single-ended circuits and push–push circuits consisting of two single-ended VCO's operating 180° out of phase, with a common output at the second harmonic frequency. Bipolar transistor VCO's are used in low-noise applications because their phase noise is lower than that of GaAs FET VCO's. With the aid of the push–push configuration, bipolar VCO's operate successfully at frequencies through Ku band.

The frequency tuning element of most VCO's is either a varactor or a YIG resonator. Varactor diodes exhibit a nonlinear capacitance versus voltage relationship and typically yield nonlinear frequency tuning characteristics. Frequency tuning can be linearized with hyperabrupt varactors or with external linearizing circuits. YIG-tuned VCO's exhibit low phase noise, linear frequency tuning, and wide bandwidths. Their main drawback is slow frequency slewing (typically 1 ms/GHz).

B. Frequency Multipliers

Frequency multiplication is an essential algebraic function used in most synthesizer architectures. The most common types of frequency multipliers are described below.

1) Diode multipliers can be divided into nonlinear capacitance circuits utilizing either varactor or step recovery diodes and nonlinear resistance circuits utilizing Schottky diodes. Nonlinear capacitance circuits can be either single-ended or push–push while nonlinear resistance circuits usually use push–push or quad diode configurations.
2) Transistor multipliers utilize bipolar transistors or FET's in either single-ended or push–push configu-

rations. Multiplication occurs as a consequence of device nonlinearities under large-signal conditions.

3) Both analog and digital PLL's can be used as multipliers. In the former the reference frequency is multiplied and the PLL serves as a narrow-band filter which attenuates the other harmonics of the reference. In the latter the reference frequency is multiplied by the division ratio of the digital frequency divider. A variable frequency multiplier can be implemented with a programmable frequency divider in the PLL.

C. Frequency Dividers

Frequency division is also an algebraic function used in many synthesizer architectures. Although several frequency division schemes are in existence, the two most common are as follows:

1) Diode dividers use either varactor or step-recovery diodes, typically connected in the push–push configuration. These circuits can be viewed as frequency multipliers operated in reverse, but their operation is based on parametric oscillations and carrier storage, respectively [1]. Division ratios other than 2 are rare.
2) Digital dividers are the most commonly used in frequency synthesizers, can have either fixed or variable (programmable) division ratios, and can be made of either silicon or GaAs. GaAs offers the advantage of higher operating frequency (15 GHz for fixed ratio dividers) but exhibits higher $1/f$ noise than silicon.

D. Mixers

Mixers fall into two categories: passive and active. Passive mixers utilize Schottky diodes in a variety of configurations. Multiple-diode mixers offer higher compression levels but also require higher levels of LO power. Active mixers utilize transistors and offer conversion gain rather than conversion loss.

E. Phase Detectors

Many types of phase detectors exist, with characteristics that are suitable for specific applications. Three types are described below.

1) A balanced mixer is often used as a phase detector in analog PLL's. It has the advantages of high-frequency operation and simplicity but its major drawback is that it exhibits relatively low isolation.
2) A sampling phase detector is used in analog PLL's where the VCO has to phase-lock to harmonics of the reference frequency. It is a balanced mixer that has an impulse generator in its LO circuit, so that an external comb generator is not required [4].
3) The phase/frequency detector is an integrated circuit used in digital PLL's [4], [10]. When the PLL is locked it acts as a phase detector; when the PLL is unlocked it generates a frequency-dependent voltage used to slew the VCO frequency into the lock-in range. Its advantages are automatic frequency acquisition and low cost while its main disadvantages are its limited operating frequency (below 100 MHz) and crossover distortion [4]. Higher frequency phase/frequency detectors have been developed (using GaAs), but to date they have not gained widespread use in low-noise applications.

F. Reference Sources

The most commonly used reference sources consist of either crystal oscillators or surface acoustic wave (SAW) oscillators. Dielectric resonator oscillators are used in some cases and atomic oscillators (e.g. rubidium or cesium) are used in applications requiring extreme frequency stability. The stability of crystal oscillators depends on the cut of the quartz crystal. Crystal oscillators using AT cut crystals can be temperature compensated, but do not offer the lowest phase noise, while SC cut crystals offer lower phase noise but must be operated in an oven. SAW oscillators use either SAW delay lines or SAW resonators (SAWR's) in the feedback circuit. The phase noise of SAWR oscillators is lower than that of SAW delay line oscillators because of the higher Q of SAW resonators. State-of-the-art SAWR oscillators have exhibited phase noise levels below -170 dBc/Hz at offset frequencies above 100 kHz [11].

G. Discriminators

A discriminator converts frequency variations to output voltage variations and serves as an essential element of FLL's. Numerous discriminator circuits have been developed over the years and open for the most widely used is shown in Fig. 8. Here the input signal is split by the power divider and applied to the two arms, one containing a passive dispersive element and the other a 90° phase shifter. The outputs of the two arms are connected to the inputs of the phase detector. Variations in input frequency are converted to phase variations in the dispersive element, which are subsequently converted to voltage variations in the phase detector. The dispersive element can be fixed (e.g. dielectric resonator, quartz crystal, delay line) or tunable (e.g. YIG filter). An enhancement of discriminator sensitivity is accomplished with carrier nulling [12], wherein most of the signal's carrier passing through the dispersive arm is canceled by a signal from a nondispersed third arm. Phase noise, however, is not canceled, resulting in larger noise side bands to the phase detector if the input power is increased. With adequate nulling, the increase in sensitivity equals one half the increase in power.

H. Amplifiers

Amplifiers have been in existence for many years and represent a mature technology. The only issue worth mentioning is that of additive phase and amplitude noise. Usually the noise performance of amplifiers is characterized by noise figure. In synthesizers for high-performance radars, however, amplifiers must also exhibit very low additive phase and amplitude noise levels at frequencies close to the carrier because this noise is a significant contributor to synthesizer performance. Typically the additive phase noise of silicon transistor amplifiers is lower than that of GaAs FET amplifiers.

VI. Future Trends

Much of the progress in frequency synthesizers will be directly influenced by advances in the state of the art of semiconductor devices. In the area of silicon semiconductor devices, present-day performance is expected to extend to higher frequencies. In GaAs technology, improvements are expected to bring both lower noise and higher frequencies. These improvements will directly impact the performance of key synthesizer components, such as amplifiers, VCO's, frequency multipliers and dividers, and reference sources. For example, the recently developed GaAs heterojunction bipolar transistor [13] was reported to operate above 20 GHz while achieving noise levels comparable to those of silicon bipolar transistors.

Diode mixers and phase detectors (including discriminators) are relatively mature technologies and can be expected to change only slightly as semiconductor technology advances. Digital phase/frequency detectors and digital frequency dividers have the potential for future improvements as a result of further developments in silicon and GaAs technologies.

Reference sources have been improving and should continue to do so with time, both through refinement and by the introduction of new types, the SAW and dielectric resonator oscillators being the most recent successful additions to the list of usable components. SAW device improvements will be only incremental, but higher Q dielectric resonators are presently being developed which will lead to lower noise oscillators.

Significant improvements are also expected in the area of direct digital synthesis, where operating frequencies are presently up to 500 MHz using GaAs devices. Further developments in this relatively new field will follow improvements in semiconductor devices.

The most dramatic improvements in frequency synthesizer technology will occur when the phase noise of GaAs devices is reduced. This will extend the state of the art in low-noise synthesis to much higher frequencies.

Finally, in all areas except those with high power levels, the development of MMIC technologies will lead to smaller, more efficient designs, higher levels of integration, and cost reductions in production.

VII. Summary

An overview of frequency synthesizers suitable for radar systems has been presented. Key radar requirements have been outlined and related to synthesizer performance. Both direct and indirect architectures have been considered.

The direct architectures described in this paper have been selected specifically for their low phase noise performance. Many classical direct architectures were not mentioned because of their lesser suitability for radar.

Indirect architectures have also been presented. It was pointed out that while their phase noise is higher than that of the lowest noise direct architectures, they are more suitable for airborne applications because of their smaller volume and lower complexity. Typically analog indirect synthesizers have lower noise than their digital counterparts. However, digital indirect synthesizers are used extensively because of their attractive features, especially automatic frequency acquisition and the capability to synthesize a large number of frequencies in a small volume.

Key synthesizer components have also been mentioned and future projections made for components that have not yet reached maturity.

References

[1] V. Manassewitsch, *Frequency Synthesizers Theory and Design*, 3rd ed. New York: Wiley, 1987.

[2] V. Kroupa, *Frequency Synthesis Theory, Design and Applications*. New York: Wiley, 1973.

[3] J. Gorski-Popiel, Ed. *Frequency Synthesis: Techniques and Applications*. New York: IEEE Press, 1975.

[4] W. F. Egan, *Frequency Synthesis by Phase Lock*. New York: Wiley, 1981.

[5] G. Jerinic, N. Gregory, and W. Murphy, "Low noise microwave oscillator design," in *Proc. 29th Annual Symp. Frequency Contr.*, 1975, pp. 248–263.

[6] F. Gardner, *Phaselock Techniques*, 2nd ed. New York: Wiley, 1979.

[7] I. Yuval, "Proper delay line discriminator design avoids common pitfalls," *Microwave Syst. News*, pp. 109–118, Dec. 1981.

[8] Z. Galani *et al.*, "Analysis and design of a single-resonator GaAs FET oscillator with noise degeneration," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1556–1565, Dec. 1984.

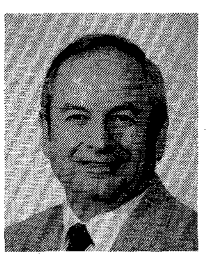
[9] D. Cheadle, "Selecting mixers for best intermod performance," *Microwaves*, pp. 48–52, Nov. 1973; also pp. 58–62, Dec. 1973.

[10] J. Crawford, "The phase/frequency detector," *RF Design*, pp. 46–57, Feb. 1985.

[11] T. E. Parker and G. K. Montress, "Low noise SAW resonator oscillators," in *Proc. 43rd Annual Symp. Frequency Contr.*, 1989, pp. 588–595.

[12] K. H. Sann, "The measurement of near-carrier noise in microwave amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-16, pp. 761–766, Sept. 1968.

[13] U. L. Rohde, "Low-noise source uses heterojunction bipolar transistor," *Microwaves & RF*, pp. 81–88, Feb. 1989.

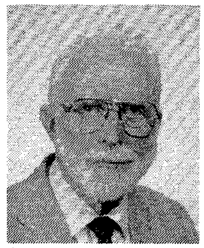


Zvi Galani (S'68–M'72–SM'82) received the B.S.E.E. degree from the Milwaukee School of Engineering in 1963 and the M.S. and Ph.D. degrees in electrical engineering from Cornell University in 1969 and 1972, respectively.

In 1963 he joined the General Electrical Company's Communication Products Department and was involved in the design of low-noise microwave sources for multichannel telecommunication systems. In 1972 he accepted the position of Senior Design Engineer with the

Raytheon Missile Systems Division Bedford Laboratories. His work consisted in the design of microwave components and subsystems for the generation and amplification of microwave signals. From 1976 to 1982 he managed the Sources and Devices Section in the Missile Microwave and Antenna Department of the Missile Guidance Laboratory. In that position he provided technical direction and took an active part in the development and design of microwave signal sources and exciters for missile seekers. In 1982 he joined the Technical Staff of the Manager of Bedford Laboratories. In that position his principal tasks have been the solution of critical production problems on major programs such as the Hawk, Patriot, Sparrow and AEGIS ER missile systems. In 1985 he was promoted to Consulting Engineer, the highest engineering level attainable at Raytheon. This designation is given in special recognition of continually outstanding achievement over a long period of time.

In January 1986 Dr. Galani joined the MTT-S Membership Services Committee as Chapter Records Chairman and served in that position until May 1990. From 1987 through 1989 he also served as the Special Articles Editor for the *MTT-S Newsletter*. In 1989 he was elected to MTT-S AdCom for the term 1990–1992 and served as AdCom Secretary in 1990. Presently he is the Chairman of the MTT-S Membership Services Committee. Dr. Galani is on the editorial board of the MTT-S TRANSACTIONS. He holds numerous patents and has authored papers on microwave sources, power FET amplifiers, and amplifier combiner circuits.



Richard A. Campbell was born in Edwardsville, IL, on May 9, 1931. He received the BA degree in 1952 from Washington University, St. Louis, MO, and the MS degree in 1954 from the University of Rochester, Rochester, NY, both in physics.

Since 1954 he has been employed by the Raytheon Company's Missile Systems Division in the design and development of radar subsystems, with particular emphasis on radar transmitters, exciters, and test equipment. His primary interests are in the generation of low-noise microwave signals for local oscillators and radar exciters, areas in which he holds several patents.